AMENDMENTS OF THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Previously presented) A circuit that corrects errors in configuration data stored on a programmable logic device, the programmable logic device comprising:

a memory in which the configuration data and error check data associated with the configuration data is stored; and

error correction circuitry coupled to at least some of the memory to analyze the configuration data stored in the memory to determine if any values have changed after initial configuration of the memory and to correct any values that have changed.

2. (Previously presented) The circuit of claim 1 wherein the error correction circuitry comprises at least one scrubbing circuit operative to:

read from the memory a portion of the configuration data and an associated portion of the error check data; and

apply an error correcting code on the portion of the configuration data and the associated portion of the error check data to determine whether at least one bit in the portion of the configuration data has an error and to correct the at least one bit that has the error.

3. (Original) The circuit of claim 2 wherein the scrubbing circuit is associated with a subset of the configuration data and an associated subset of the error check data.

4. (Original) The circuit of claim 1 wherein:

the configuration data is stored in an array of representative rows and representative columns of cells, each cell storing one bit of the configuration data; and

the error check data is stored in a last representative column of cells and a last representative row of cells in the array, each cell storing one bit of the error check data.

5. (Original) The circuit of claim 4 wherein the error correction circuitry comprises:

first circuitry having an input operative to receive data from each cell in a representative row of the array and an output, the first circuitry generating a first parity for the data in the representative row at the output;

second circuitry having an input operative to receive data from each cell in a representative column of the array and an output, the second circuitry generating a second parity for the data in the representative column at the output;

third circuitry having a first input operative to receive the output of the first circuitry, having a second input operative to receive the output of the second circuitry, and an output, the third circuitry sending a signal at the output indicative of whether an error has occurred in a cell in the representative row and the representative column based on the first parity and the second parity; and

fourth circuitry having a first input operative to receive the output of the third circuitry, a second input operative to receive data from the cell in the representative row and the representative column, and an

output, the fourth circuitry sending a signal at the output having a correct value.

6. (Original) The circuit of claim 5 wherein the correct value is:

the data from the cell when the output of the first logic gate indicates that no error has occurred; and

the complement of the data from the cell when the output of the first logic gate indicates that the error has occurred.

7. (Original) The circuit of claim 5 further comprising fifth circuitry operative to write the correct value into the cell.

8. (Original) The circuit of claim 4 wherein the error correction circuitry comprises:

first circuitry having an input operative to receive data from all but one cell in a representative row of the array and an output, the first circuitry generating a first parity for the data from all but the one cell in the representative row at the output;

second circuitry having an input operative to receive data from all but the one cell in a representative column of the array and an output, the second circuitry generating a second parity for the data from all but the one cell in the representative column at the output; and

third circuitry having a first input operative to receive the output of the first circuitry, a second input operative to receive the output of the second circuitry, a third input operative to receive data from the one cell, and an output, the third circuitry generating a correct value at the output.

9. (Original) The circuit of claim 8 further comprising fourth circuitry operative to write the correct value into the one cell.

10. (Original) The circuit of claim 1 wherein each bit of the configuration data is stored in a first cell, a second cell, and a third cell in the memory.

11. (Original) The circuit of claim 10 wherein the error correction circuitry generates as output a same bit value that is stored in at least two of the first cell, the second cell, and the third cell.

12. (Original) The circuit of claim 11 wherein the error correction circuitry comprises circuitry having a first input operative to receive a bit from the first cell, a second input operative to receive a bit from the second cell, a third input operative to receive a bit from the third cell, and an output, the circuitry generating a correct bit value at the output.

13. (Original) The circuit of claim 12 further comprising second circuitry operative to write the correct bit value into at least one of the first cell, the second cell, and the third cell.

14. (Original) The circuit of claim 1 further comprising:

a resistive element coupled to an output of the error correction circuitry; and

a capacitive load coupled to the resistive element, wherein the resistive element and the capacitive load are operative to reduce static hazards associated with the error correction circuitry.

15. (Original) The circuit of claim 14 wherein the resistive element is one of a polysilicon wire, a current starved pass gate, and a current starved inverter.

16. (Original) A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 1 coupled to the processing circuitry and the memory.

17. (Original) A printed circuit board on which is mounted a programmable logic device as defined in claim 16.

18. (Original) The printed circuit board defined in claim 17 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

19. (Original) The printed circuit board defined in claim 17 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

20. (Previously presented) A circuit that corrects errors in configuration data stored on a programmable logic device, the programmable logic device comprising:

a memory in which the configuration data and error check data associated with the configuration data are stored; and

at least one scrubber coupled to the memory and operative to:

read from the memory a portion of the configuration data and an associated portion of the error check data, and

apply an error correcting code on the portion of the configuration data and the portion of the error check data to determine whether at least one bit in the portion of the configuration data has an error and to correct the at least one bit that has the error.

21. (Original) The circuit of claim 20 further comprising one scrubber associated with the configuration data and the error check data.

22. (Original) The circuit of claim 20 further comprising more than one scrubber each associated with a subset of the configuration data and an associated subset of the error check data.

23. (Original) The circuit of claim 20 wherein the error correcting code is one of a Hamming Code, a Reed-Solomon Code, and a Product Code.

24. (Original) A circuit that corrects errors in configuration data stored on a programmable logic device comprising:

a memory array of representative rows and representative columns of cells in which the configuration data and error check data associated with the configuration data are stored;

first circuitry having an input operative to receive data from each cell in a representative row of the array and an output, the first circuitry generating a first parity for the data in the representative row at the output;

second circuitry having an input operative to receive data from each cell in a representative column of the array and an output, the second circuitry generating a second parity for the data in the representative column at the output;

third circuitry having a first input operative to receive the output of the first circuitry, having a second input operative to receive the output of the second circuitry, and an output, the third circuitry sending a signal at the output indicative of whether an error has occurred in a cell in the representative row and the representative column based on the first parity and the second parity; and

fourth circuitry having a first input operative to receive the output of the third circuitry, a second input operative to receive data from the cell in the representative row and the representative column, and an output, the fourth circuitry sending a signal at the output having a correct value.

25. (Original) The circuit of claim 24 wherein the correct value is:

the data from the cell when the output of the first logic gate indicates that no error has occurred; and

the complement of the data from the cell when the output of the first logic gate indicates that an error has occurred.

26. (Original) The circuit of claim 24 further comprising fifth circuitry operative to write the correct value into the cell.

27. (Original) A circuit that corrects errors in configuration data stored on a programmable logic device comprising:

a memory array of representative rows and representative columns of cells in which the configuration data and error check data associated with the configuration data are stored;

first circuitry having an input operative to receive data from all but one cell in a representative row of the array and an output, the first circuitry generating a first parity for the data from all but the one cell in the representative row at the output;

second circuitry having an input operative to receive data from all but the one cell in a representative column of the array and an output, the second circuitry generating a second parity for the data from all but the one cell in the representative column at the output; and

third circuitry having a first input operative to receive the output of the first circuitry, a second input operative to receive the output of the second circuitry, a third input operative to receive data from the one cell, and an output, the third circuitry generating a correct value at the output.

28. (Original) The circuit of claim 27 further comprising fourth circuitry operative to write the correct value into the one cell.

29-36. (Cancelled)

37. (Currently amended) A method for correcting errors in configuration data stored on a programmable logic device comprising:

generating and storing in a memory of the programmable logic device error check data associated with the configuration data ~~in a memory~~;

reading a portion of the configuration data and an associated portion of the error check data;

determining if an error has occurred based on the portion of the configuration data and the associated portion of the error check data; and

correcting the portion of the configuration data in response to the determining.

38. (Original) The method of claim 37 wherein the portion of the configuration data is at least one representative column of cells in the memory.

39. (Original) The method of claim 37 wherein the portion of the configuration data is at least one partial representative column of cells in the memory.

40. (Original) The method of claim 37 wherein the portion of the configuration data is at least two partial representative columns of cells in the memory that are physically contiguous.

41. (Original) The method of claim 37 wherein the portion of the configuration data is at least two partial representative columns of cells in the memory that are physically non-contiguous.

42. (Original) The method of claim 37 wherein the determining comprises applying an error correcting code on the portion of the configuration data and the associated portion of the error check data.

43. (Original) The method of claim 42 wherein the error correcting code is one of a Hamming Code, a Reed-Solomon Code, and a Product Code.

44. (Original) The method of claim 37 wherein the correcting comprises writing the corrected portion of the configuration data into the memory.

45. (Currently amended) A method for correcting errors in configuration data stored on a programmable logic device comprising:

generating and storing on the programmable logic device a parity bit associated with each representative row and each representative column of memory cells in which the configuration data is stored;

computing a first parity on a given representative row of memory cells;

computing a second parity on a given representative column of memory cells;

determining if an error has occurred in a cell in the given representative row and the given representative column based on the first parity and the second parity; and

correcting the data in the cell in response to the determining.

46. (Original) The method of claim 45 wherein the parity bit associated with each representative row and each representative column is a logic value that allows the associated representative row or representative column to have one of even parity and odd parity.

47. (Original) The method of claim 45 wherein correcting the data comprises inverting the logic of the data in the cell for output.

48. (Original) The method of claim 45 wherein correcting the data comprises writing the corrected data into the cell.

49. (Currently amended) A method for correcting errors in configuration data stored on a programmable logic device comprising:

generating and storing on the programmable logic device a parity bit associated with each representative row and each representative column of memory cells in which the configuration data is stored;

computing a first parity on all but one cell in a given representative row of memory cells;

computing a second parity on all but the one cell in a given representative column of memory cells; and

generating a correct value for the data in the one cell based on the first parity, the second parity, and data in the one cell.

50. (Original) The method of claim 49 wherein the parity bit associated with each representative row and each representative column is a logic value that allows the associated representative row or representative column to have one of even parity and odd parity.

51. (Original) The method of claim 49 further comprising writing the corrected data into the one cell.

52-53. (Cancelled)